Kishal Bipin Tandel
23MS115
February 13, 2026

Report 2

Instructors:
Satyabrata Raj
Goutam D. Mukherjee

PH3204: Electronics Laboratory

Abstract

In this experiment, the static characteristics of an npn Bipolar Junction Transistor (BJT) are studied in the common emitter (CE) configuration. The input characteristics, defined by the variation of base current I_B with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}, and the output characteristics, defined by the variation of collector current I_C with V_{CE} at constant I_B, are obtained experimentally. The current amplification property of the transistor is examined. From the output characteristics, the DC current gain β is calculated.

Contents

1. Introduction

The Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device that plays a central role in analog electronics. It is widely used in amplification, switching, oscillators, waveform generators, and digital logic circuits. The name "bipolar" arises from the fact that both electrons and holes participate in current conduction.

Structurally, a BJT consists of two *pn* junctions formed by sandwiching a thin region of one type of semiconductor between two regions of the opposite type. Depending on the arrangement, the transistor may be of type *npn* or *pnp*. In this experiment, we study an *npn* transistor, which is more commonly used due to higher electron mobility and better performance.

The transistor has three terminals:

1. Emitter (E) – heavily doped region that injects charge carriers.
2. Base (B) – very thin and lightly doped region.
3. Collector (C) – moderately doped and physically larger region that collects carriers.

When properly biased, a small base current controls a much larger collector current, enabling amplification. The present experiment focuses on understanding this behavior quantitatively through characteristic curves.

1.1 Aim

To study the input and output characteristics of an NPN Bipolar Junction Transistor in the common emitter (CE) configuration and to determine its DC current gain β.

1.2 Components and Instruments

1. Power supply, 2 Nos : $0 \sim 15$ V
2. R_B, $R_C = 1.0$ kΩ, 2 Nos
3. $R_B = 220\ \Omega$, 1 No
4. 1.0 kΩ Potentiometer, 1.0 W
5. NPN Transistor = 1 No, CL100 / SL100 [CK100 / SK100 – PNP (equivalent) transistors]
6. Breadboard = 1 No
7. Two DT-830D multimeters for current measurements. One 8007 multimeter with probe for voltage measurements.
8. Single stand wires = 6 Nos

2. Theory

2.1 Basic Operation of BJT

A BJT contains two *pn* junctions: the base-emitter (BE) junction and the base-collector (BC) junction. For normal active operation:

1. The base-emitter junction is forward biased.
2. The collector-base junction is reverse biased.

In an NPN transistor, forward biasing the BE junction injects electrons from the emitter into the base. Since the base is thin and lightly doped, most of these electrons diffuse across the base and are swept into the collector by the reverse-biased BC junction. Only a small fraction recombines in the base, producing the base current I_B.
The three currents are related by:

$$I_E = I_C + I_B$$

The common-base current gain is defined as:

$$\alpha = \frac{I_C}{I_E}, \quad \alpha < 1$$

Using $I_E = I_C + I_B$,

$$I_C = \alpha(I_C + I_B)$$

which leads to

$$I_C = \beta I_B$$

where

$$\beta = \frac{\alpha}{1-\alpha}$$

The parameter β is called the **DC current gain** of the transistor and typically lies between 100 and 200.

2.2 Common Emitter Configuration

In the common emitter (CE) configuration, the emitter terminal is common to both input and output circuits. The input is applied between base and emitter, and the output is taken between collector and emitter. Input variables are $V_{BE}, \quad I_B$ and output variables are $V_{CE}, \quad I_C$.

The CE configuration is widely used because:

1. It provides high current gain (β).

2. It provides significant voltage gain.

3. It offers moderate input and output impedances.

The CE configuration operates in three regions:

1. Cutoff region: $I_B \approx 0$, $I_C \approx 0$.

2. Active region: $I_C = \beta I_B$ (amplifier region).

3. Saturation region: Both junctions forward biased, V_{CE} small.

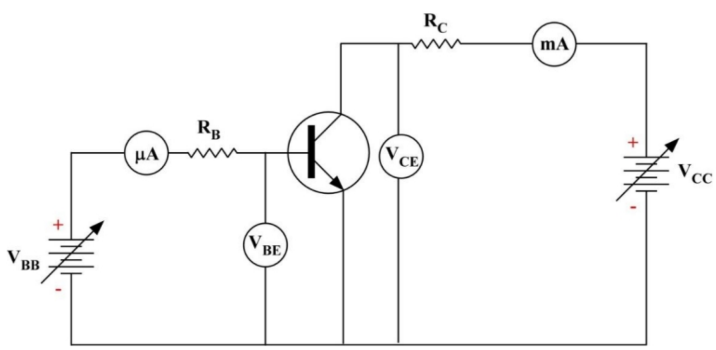

Figure 1: Circuit for transistor characteristics in CE configuration

2.2.1 CE Input Characteristics

The input characteristic is the graph of I_B versus V_{BE} at constant V_{CE}.

The base-emitter junction behaves like a forward-biased diode. Therefore, the base current approximately follows the diode equation:

$$I_B = I_S \left(e^{\frac{V_{BE}}{\eta V_T}} - 1 \right) \tag{2.2.1.1}$$

where:

- I_S is reverse saturation current
- η is ideality factor
- $V_T = \frac{kT}{q} \approx 25\,\text{mV}$ at room temperature

For silicon transistors, significant conduction begins near:

$$V_{BE} \approx 0.6 - 0.7\,\text{V}$$

Thus, the input characteristic resembles that of a diode. As V_{CE} increases slightly, the curve shifts marginally due to base-width modulation (Early effect).

2.2.2 CE Output Characteristics

The output characteristic is the graph of I_C versus V_{CE} at constant I_B.

For a fixed base current:

$$I_C \approx \beta I_B$$

In the active region, I_C is nearly independent of V_{CE}, producing almost horizontal characteristic curves.

At low V_{CE} (typically < 0.7 V), the transistor enters saturation and I_C increases rapidly with V_{CE}. In practice, due to the Early effect, I_C slightly increases with V_{CE} even in the active region.

The DC current gain at a given V_{CE} is:

$$\beta = \frac{I_C}{I_B}$$

3. Observation Table

3.1 CE Input Characteristics

Sl. No.	$V_{CE} = 2$ V		$V_{CE} = 3$ V		$V_{CE} = 4$ V	
	V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)
1	0.05	0	0.05	0	0.04	0
2	0.23	0	0.24	0	0.21	0
3	0.31	0	0.30	0	0.29	1
4	0.43	3	0.39	1	0.37	3
5	0.52	4	0.48	2	0.46	4
6	0.61	13	0.59	3	0.56	7
7	0.66	51	0.66	66	0.64	82
8	0.70	102	0.67	94	0.66	157
9	0.73	163	0.68	171	0.66	267
10	0.75	234	0.69	250	0.67	331
11	0.76	306	0.70	336	0.67	397
12	0.76	368	0.70	440	0.68	483
13	0.76	439	0.71	518	0.68	552
14	0.76	557	0.71	564	0.68	593

Table 1: CE Input Characteristics

3.1.1 Graph

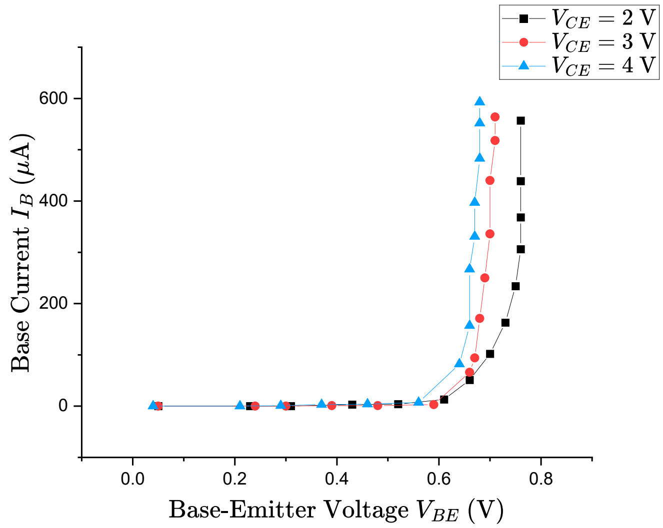

Figure 2: CE Input Characteristics

3.1.2 Discussion

The input characteristics of the NPN transistor in common emitter (CE) configuration were studied by plotting the base current I_B versus the base–emitter voltage V_{BE} at constant collector–emitter voltages $V_{CE} = 2\,\text{V}, 3\,\text{V}$, and $4\,\text{V}$.

From the plotted curves, it is observed that the input characteristic resembles that of a forward biased p–n junction diode. For small values of V_{BE} (below approximately 0.55–0.6 V), the base current I_B remains nearly zero. This is because the base–emitter junction has not yet reached its threshold voltage.

As V_{BE} approaches approximately 0.6–0.7 V, the base current increases rapidly. This sharp rise confirms the exponential relationship between I_B and V_{BE}, which follows the diode equation given by Eq. (2.2.1.1). Thus, a small increase in V_{BE} produces a large increase in I_B, which is clearly evident from the graph.

When comparing the three curves corresponding to $V_{CE} = 2\,\text{V}, 3\,\text{V}$, and $4\,\text{V}$, a slight shift in the characteristics is observed. With increase in V_{CE}, the curves shift slightly towards the left (or equivalently downward). This indicates that for the same base current, a slightly lower value of V_{BE} is required at higher V_{CE}.

This behavior can be explained by the Early effect (base width modulation). As V_{CE} increases, the collector–base junction reverse bias increases, causing the depletion region at the collector side to widen. This reduces the effective base width. Due to the reduced base width, recombination of charge carriers in the base decreases. Consequently, a smaller base current is sufficient to maintain conduction.

However, the shift in the curves is very small, indicating that the input characteristic is primarily governed by the forward biased base–emitter junction and is only weakly influenced by the collector voltage.

The exponential nature of the curves confirms that the base–emitter junction behaves like a silicon diode with a threshold voltage around 0.6–0.7 V, which is in good agreement with theoretical expectations.

3.2 CE Output Characteristics

Sl. No	$I_B = 10\ \mu$A		$I_B = 20\ \mu$A		$I_B = 30\ \mu$A		$I_B = 40\ \mu$A	
	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
2	0.07	0.04	0.01	0.07	0.02	0.24	0.01	0.17
3	0.21	0.17	0.02	0.09	0.03	0.46	0.02	0.29
4	0.26	0.20	0.04	0.18	0.05	0.63	0.03	0.46
5	0.35	0.32	0.05	0.22	0.06	0.85	0.04	0.63
6	0.47	0.38	0.06	0.36	0.07	1.23	0.05	0.94
7	0.55	0.43	0.07	0.38	0.08	1.47	0.06	1.36
8	0.62	0.51	0.08	0.48	0.09	1.83	0.07	1.87
9	0.65	0.53	0.09	0.61	0.10	2.21	0.08	2.31
10	0.69	0.58	0.10	0.69	0.11	2.60	0.09	2.83
11	0.79	0.74	0.11	0.78	0.12	3.17	0.10	3.75
12	0.91	0.82	0.12	0.90	0.13	3.69	0.11	4.24
13	0.97	0.86	0.13	1.09	0.14	4.03	0.12	5.13
14	1.13	0.99	0.14	1.24	0.15	4.39	0.15	5.60
15	1.24	1.14	0.15	1.63	0.22	4.87	0.16	6.13
16	1.33	1.18	0.16	1.91	0.55	5.09	0.19	6.23
17	1.41	1.26	0.17	2.33	0.24	5.10	0.20	6.31
18	1.54	1.44	0.21	2.60	0.34	5.13	0.21	6.57
19	1.77	1.57	0.27	3.14	0.35	5.16	0.22	6.65
20	1.84	1.63	0.32	3.56	0.87	5.23	0.24	6.77
21	1.91	1.64	0.44	3.64	2.01	5.34	0.43	6.81
22	2.05	1.71	0.57	3.63	3.39	5.27	0.54	6.84
23	2.13	1.72	0.63	3.64	4.44	5.36	0.83	6.86
24	2.24	1.75	1.13	3.65	4.77	5.26	1.74	6.93
25	2.32	1.82	2.53	3.71	5.30	5.33	2.56	6.99
26	2.91	1.81	3.62	3.63	5.98	5.34	3.66	6.88
27	4.55	1.74	5.09	3.70	6.23	5.27	4.78	6.93
28	5.41	1.78	6.11	3.71	6.87	5.38	5.65	6.95
29	6.33	1.79	6.20	3.73	7.60	5.34	6.68	6.90
30	7.25	1.77	7.10	3.74	8.54	5.27	7.72	6.91
31	8.74	1.80	8.33	3.70	9.32	5.33	8.81	6.87
32	9.55	1.78	9.45	3.73	9.89	5.34	9.76	6.94

Table 2: CE Output Characteristics

3.2.1 Graph

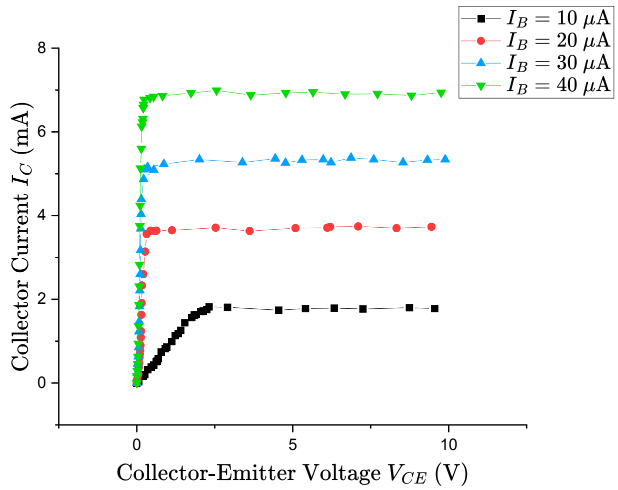

Figure 3: CE Output Characteristics

3.2.2 Discussion

The output characteristics of the NPN transistor in common emitter (CE) configuration were obtained by plotting the collector current I_C versus collector–emitter voltage V_{CE} for different fixed values of base current I_B (10 μA, 20 μA, 30 μA, and 40 μA).

From the graph, three distinct regions of operation are observed:

a) Saturation Region

At very small values of V_{CE} (approximately below 0.7 V), the collector current increases rapidly with increase in V_{CE}. In this region, both the base–emitter and base–collector junctions are forward biased. The transistor operates in saturation and does not follow the linear amplification relation $I_C = \beta I_B$.

b) Active Region

For V_{CE} greater than approximately 1 V, the collector current becomes nearly constant for a fixed I_B. This region is known as the active region. In this region,

$$I_C \approx \beta I_B$$

The curves corresponding to different base currents are nearly horizontal and approximately parallel, indicating that I_C depends primarily on I_B and only weakly on V_{CE}.

A slight upward slope in the curves is observed even in the active region. This is due to the Early effect (base width modulation), which causes a small increase in collector current with increasing V_{CE}.

c) Cutoff Region

When $I_B = 0$, the transistor would ideally be in cutoff and I_C would be nearly zero. Although this case was not explicitly plotted, it is understood from transistor theory.

3.2.3 Determination of Current Gain β

The following table shows the DC current gain β at $V_{CE} = 5$ V as caluclated from the output characteristics graph.

Sl. No.	I_B (μA)	I_C (mA)	$\beta = \frac{I_C}{I_B}$
1	10	1.76	176.0
2	20	3.71	185.5
3	30	5.28	176.0
4	40	6.93	173.3

Table 3: DC Current gain β values

Average DC current gain $\beta \approx 178$.

The values are reasonably consistent, confirming that the transistor operates properly in the active region. The slight variation in β with I_B indicates that β is not perfectly constant but depends weakly on operating conditions.

4. Sources of Error

4.1 Systematic Errors

1. **Instrument Calibration Error:** Multimeters may have inherent calibration errors that cause consistent deviation in current or voltage measurements.

2. **Internal Resistance of Meters:** Multimeter internal resistance can affect current flow, especially in low-current measurements such as base current.

3. **Power Supply Fluctuations:** Variations in DC supply voltage can affect V_{CE} and I_B, leading to systematic shifts in readings.

4. **Temperature Variation:** Transistor parameters such as β and V_{BE} are temperature dependent. Increase in temperature reduces V_{BE} and increases leakage currents.

5. **Contact Resistance:** Poor connections in breadboard and connecting wires introduce additional resistance.

6. **Resolution Limit of Multimeter:** Limited decimal precision restricts measurement accuracy.

4.2 Random Errors

1. **Electrical Noise:** Fluctuations in readings due to environmental electromagnetic interference.

2. **Reading Fluctuations:** Slight instability in digital display during measurement.

3. **Manual Adjustment Errors:** Difficulty in precisely setting I_B to exact desired values.

4. **Thermal Drift During Experiment:** Continuous operation may heat the transistor, changing current values slightly over time.

5. Results

1. The input characteristics showed diode-like exponential behavior of the base–emitter junction.
2. The output characteristics clearly exhibited saturation and active regions.
3. The collector current remained nearly constant with increasing V_{CE} in the active region.
4. The DC current gain β at $V_{CE} = 5\,\text{V}$ was calculated for different base currents.
5. The average current gain was found to be $\beta_{\text{avg}} \approx 178$.

6. Conclusion

The characteristics of the NPN transistor in common emitter configuration were successfully studied. The input characteristics confirmed that the base–emitter junction behaves like a forward biased silicon diode with threshold voltage around 0.6–0.7 V.

The output characteristics demonstrated the presence of saturation and active regions. In the active region, the collector current was found to be approximately proportional to the base current, validating the relation $I_C = \beta I_B$.

The calculated average current gain $\beta \approx 178$ falls within the expected range for the transistor type used, confirming proper device operation. Minor deviations from ideal behavior were attributed to the Early effect and experimental uncertainties.

Directions for Improvement

- Use regulated and stabilized power supplies to minimize voltage fluctuations.
- Perform the experiment at controlled temperature conditions to reduce thermal drift.
- Use precision digital multimeters with higher resolution for low-current measurement.
- Ensure tight and clean connections to reduce contact resistance.
- Allow sufficient cooling time between measurements to prevent heating effects.
- Repeat measurements multiple times and use averaged values for improved accuracy.

References

1. R. L. Boylestad and L. Nashelsky, *Electronic Devices and Circuit Theory*, 11th ed. New Delhi, India: Pearson Education, 2013.
2. A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York, USA: Oxford University Press, 2015.
3. B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*, 7th ed. Noida, India: Pearson Education, 2015.